What Is Claimed Is:

1. A top metal level capacitor for integrated circuits comprising:

a bottom electrode, said bottom electrode positioned over a top metal level and coupled to a first interconnect of said top metal level;

a capacitor dielectric coupled to said bottom electrode;

a top electrode coupled to said capacitor dielectric; and

sidewalls positioned at a perimeter of said top metal level capacitor; said sidewalls coupled to said top metal level, said bottom electrode, said capacitor dielectric, and a portion of said top electrode;

wherein said top electrode is coupled to a second interconnect of said top metal level.

2. The top metal level capacitor of Claim 1 wherein the capacitor dielectric is comprised of a high-k material.

3. The top metal level capacitor of Claim 2 wherein said capacitor dielectric is TaO_X.

4. The top metal level capacitor of Claim 1 wherein said bottom electrode is comprised of a layer of TaN and a layer of TiN.

5. The top metal level capacitor of Claim 1 wherein said top electrode is comprised of a layer of TiN and a layer of TaN.

6. The top metal level capacitor of Claim 1 wherein said sidewalls are comprised of SiN.

7. The top metal level capacitor of Claim 1 wherein said first interconnect and said second interconnect are comprised of Cu.

8. The top metal level capacitor of Claim 1 wherein said first interconnect is coupled to a power supply rail.

9. The top metal level capacitor of Claim 1 wherein said second interconnect is coupled to GND.

10. The top metal level capacitor of Claim 1 wherein said top metal level capacitor is a decoupling capacitor from a supply voltage to ground.

11. A top metal level capacitor for integrated circuits comprising:

a bottom electrode comprised of a layer of TaN and a layer of TiN, said bottom electrode positioned over a top metal level and coupled to a first interconnect of said top metal level;

a capacitor dielectric comprised of TaO_X coupled to said bottom electrode;

a top electrode comprised of a layer of TiN and a layer of TaN coupled to said capacitor dielectric; and

sidewalls comprised of SiN positioned at a perimeter of said top metal level capacitor; said sidewalls coupled to said top metal level, said bottom electrode, said capacitor dielectric, and a portion of said top electrode;

wherein said layer of TaN of said top electrode is coupled to a second interconnect of said top metal level, said first interconnect is coupled to a supply voltage and is comprised of copper, and said second interconnect is coupled to ground and is comprised of copper.

12. A method of fabricating a top metal level capacitor comprising:

providing a semiconductor body having a plurality of metal interconnect levels including a top metal level, said top metal level having a first interconnect and a second interconnect;

forming a bottom electrode over said top metal level, said bottom electrode coupled to said first interconnect;

forming a capacitor dielectric over said bottom electrode;

forming a first level top electrode over said capacitor dielectric;

forming sidewalls at a perimeter of said top metal level capacitor; said sidewalls coupled to said top metal level, said bottom electrode, said capacitor dielectric, and at least a portion of said first level top electrode; and

forming a second level top electrode coupled to said first level top electrode and said second interconnect.

13. The method of Claim 12 wherein said bottom electrode is comprised of a layer of TaN and a layer of TiN.

14. The method of Claim 12 wherein said capacitor dielectric is comprised of a high-k dielectric material.

15. The method of Claim 14 wherein said capacitor dielectric is comprised of TaO_X.

16. The method of Claim 12 wherein said first level top electrode is TiN and said second level top electrode is comprised of TaN.

17. The method of Claim 12 wherein said sidewalls are comprised of SiN.

18. The method of Claim 12 wherein said first interconnect and said second interconnect are comprised of Cu.

19. The method of Claim 12 wherein said first interconnect and said second interconnect are power and ground rails.

20. A method of fabricating a top metal level capacitor comprising:

providing a semiconductor body having a plurality of metal interconnect levels including a top metal level, said top metal level having a first interconnect and a second interconnect;

forming a bottom electrode over said top metal level, said bottom electrode coupled to said first interconnect;

forming a capacitor dielectric over said bottom electrode;

forming sidewalls at a perimeter of said top metal level capacitor; said sidewalls coupled to said top metal level, said bottom electrode, and said capacitor dielectric; and

forming a top electrode coupled to said capacitor dielectric and said second interconnect.

21. The method of Claim 20 wherein said bottom electrode is comprised of a layer of TaN and a layer of TiN.

22. The method of Claim 20 wherein said capacitor dielectric is comprised of a high-k dielectric material.

23. The method of Claim 22 wherein said capacitor dielectric is comprised of TaO_X.

24. The method of Claim 20 wherein said top electrode is comprised of a layer of TiN and a layer of TaN.

25. The method of Claim 20 wherein said top electrode is comprised of a layer of TiN.

26. The method of Claim 20 wherein said top electrode is comprised of a layer of TaN.

27. The method of Claim 20 wherein said sidewalls are comprised of SiN.

28. The method of Claim 20 wherein said first interconnect and said second interconnect are comprised of Cu.

29. The method of Claim 20 wherein said first interconnect and said second interconnect are power and ground rails.

30. A method of fabricating a top metal level capacitor on a semiconductor wafer comprising:

providing a semiconductor body having a plurality of metal interconnect levels including a top metal level, said top metal level having a first interconnect and a second interconnect;

forming a layer of bottom electrode material over said top metal level;

forming a layer of capacitor dielectric material over said layer of bottom electrode material;

annealing said layer of capacitor dielectric material;

forming a first layer of top electrode material over said semiconductor wafer;

etching said semiconductor wafer using a first mask to form a material stack; said material stack including a bottom electrode coupled to said first interconnect, a capacitor dielectric coupled to said bottom electrode, and a partial first layer of top electrode coupled to said capacitor dielectric;

forming a layer of insulative material over said semiconductor wafer;

etching said layer of insulative material to form sidewalls at a perimeter of said material stack;

forming a second layer of top electrode material over said semiconductor wafer; and

etching said second layer of top electrode material using a second mask to form a complete top electrode coupled to said partial first layer of top electrode and said second interconnect.

31. The method of Claim 30 further comprising forming a protective overcoat, including an etch stop layer, over said semiconductor wafer.

32. The method of Claim 30 wherein said bottom electrode is comprised of a layer of TaN and a layer of TiN.

33. The method of Claim 30 wherein said capacitor dielectric is comprised of a high-k dielectric material.

34. The method of Claim 33 wherein said capacitor dielectric is comprised of TaO_X.

35. The method of Claim 30 wherein said partial top electrode is comprised of TiN and said complete top electrode is comprised of TaN.

36. The method of Claim 30 wherein said sidewalls are comprised of SiN.

37. The method of Claim 30 wherein said first interconnect and said second interconnect are comprised of Cu.

38. The method of Claim 30 wherein said first interconnect and said second interconnect are power and ground rails.

39. The method of Claim 30 wherein said step of etching said semiconductor wafer to from a material stack comprises:

forming a layer of photoresist over said semiconductor wafer;

patterning said layer of photoresist using said first mask;

etching said layer of photoresist to form a photoresist pattern;

etching said first layer of top electrode material, said annealed layer of capacitor dielectric material, and said layer of bottom electrode material using said photoresist pattern; and

ashing said photoresist pattern.

40. The method of Claim 30 wherein said step of etching said second layer of top electrode material comprises:

forming a layer of photoresist over said semiconductor wafer;

patterning said layer of photoresist using said second mask;

etching said layer of photoresist to form a photoresist pattern;

etching said second layer of top electrode material using said photoresist pattern; and

ashing said photoresist pattern.

41. A method of fabricating a top metal level capacitor on a semiconductor wafer comprising:

providing a semiconductor body having a plurality of metal interconnect levels including a top metal level, said top metal level having a first interconnect and a second interconnect;

forming a layer of bottom electrode material comprising a layer of TaN and a layer of TiN over said top metal level;

forming a layer of capacitor dielectric material comprising a layer of TaO_x over said layer of bottom electrode material;

annealing said layer of TaO_x to change it to a layer of higher oxygen content TaO_X;

forming a first layer of top electrode material comprising TiN over said semiconductor wafer;

etching said semiconductor wafer using a first mask to form a material stack; said material stack including a bottom electrode coupled to said first interconnect, a capacitor dielectric coupled to said bottom electrode, and a partial first layer of top electrode coupled to said capacitor dielectric;

forming a layer of insulative material comprising SiN over said semiconductor wafer;

etching said layer of SiN to form sidewalls at a perimeter of said material stack;

forming a second layer of top electrode material comprising TaN over said semiconductor wafer; and

etching said second layer of top electrode material using a second mask to form a complete top electrode coupled to said partial first layer of top electrode and said second interconnect.

42. The method of claim 41 further comprising forming a protective overcoat comprising SiO_X and including an etch stop layer comprising SiC over said semiconductor wafer.

43. A top metal level capacitor for integrated circuits comprising:

a bottom electrode, said bottom electrode positioned over a top metal level and coupled to a first interconnect of said top metal level;

a capacitor dielectric coupled to said bottom electrode;

sidewalls positioned at a perimeter of said top metal level capacitor; said sidewalls coupled to said top metal level, said bottom electrode and said capacitor dielectric; and

a top electrode coupled to said capacitor dielectric and to a second interconnect of said top metal level.

44. The top metal level capacitor of Claim 43 wherein the capacitor dielectric is comprised of a high-k material.

45. The top metal level capacitor of Claim 44 wherein said capacitor dielectric is TaO_X.

46. The top metal level capacitor of Claim 43 wherein said bottom electrode is comprised of a layer of TaN and a layer of TiN.

47. The top metal level capacitor of Claim 43 wherein said top electrode is comprised of a layer of TaN.

48. The top metal level capacitor of Claim 43 wherein said sidewalls are comprised of SiN.

49. The top metal level capacitor of Claim 43 wherein said first interconnect and said second interconnect are comprised of Cu.

50. The top metal level capacitor of Claim 43 wherein said first interconnect is coupled to a power supply rail.

51. The top metal level capacitor of Claim 43 wherein said second interconnect is coupled to GND.

52. The top metal level capacitor of Claim 43 wherein said top metal level capacitor is a decoupling capacitor from a supply voltage to ground.

53. The top metal level capacitor of Claim 43 wherein said top electrode is comprised of a layer of TiN.